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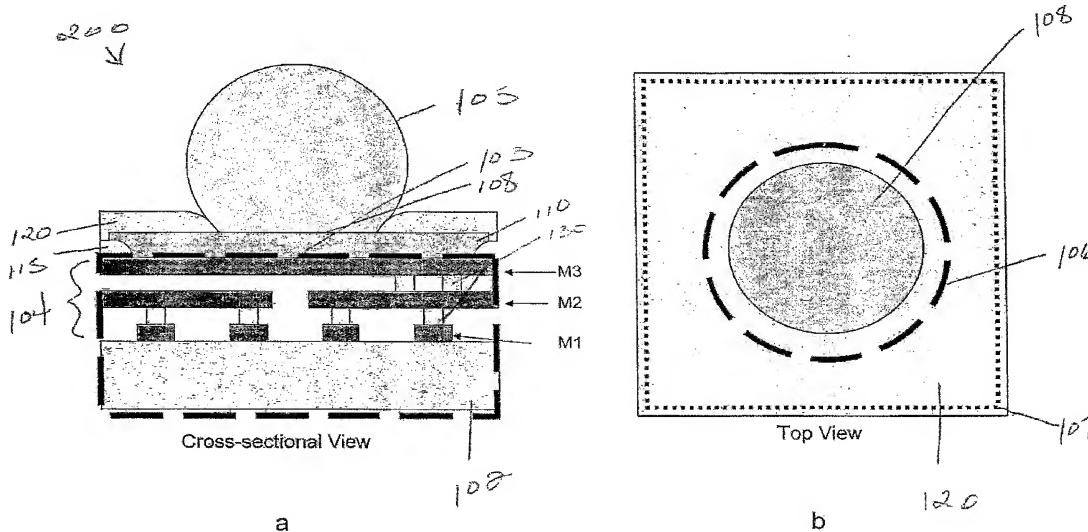
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(54) Title: SYSTEM AND METHOD TO REDUCE METAL SERIES RESISTANCE OF BUMPED CHIP

UBM Layer Covering Standard Top Metal Layer



(57) Abstract: Provided herein, in accordance with one aspect of the present invention, are exemplary embodiments of semiconductor chips having low metallization series resistance. In one embodiment, the semiconductor chip comprises a semiconductor substrate and a metallization structure formed on the semiconductor substrate; an under bump metallurgy ("UBM") structure layer formed over the metallization structure; and a bump formed over said UBM layer; wherein the largest linear dimension of said UBM layer is larger than the diameter of said bump.

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